What Is Claimed Is:

1. An MRAM memory array, comprising:

a global word line;

a global bit line;

a plurality of word lines crossing the global bit line;

a plurality of bit lines crossing the global word line;

a plurality of first switches, each of the plurality of first switches being coupled to the global word line and one or more of the bit lines;

a plurality of second switches, each of the plurality of second switches being coupled to the global bit line and one or more of the word lines; and

a plurality of magnetic tunnel junction memories including:

a pinned layer;

a free layer;

and a non-magnetic layer located between the pinned layer and the free layer; each of the plurality of magnetic tunnel junction memories being positioned at a crossing point of a bit line and a word line, each of the plurality of magnetic tunnel junction memories being connected between the first switch at the corresponding crossing bit line and the second switch at the corresponding crossing word line.

2. The MRAM memory array as claimed in claim 1, wherein the total number of switches is equal to the total number of the plurality of word lines and the plurality of bit lines.

3. The MRAM memory array as claimed in claim 1, wherein the number of the magnetic tunnel junction memories is the product of the numbers of the plurality of word lines and the number of the plurality of bit lines.

4. The MRAM memory array as claimed in claim 1, wherein the first switch includes:

a first terminal;

a control gate coupled to the global word line; and

a second terminal coupled to the corresponding one of the plurality of bit lines.

5. The MRAM memory array as claimed in claim 1, wherein the second switch includes:

a first terminal;

a control gate coupled to the global bit line; and

a second terminal coupled to one of the plurality of word lines.

6. The MRAM memory array as claimed in claim 1, wherein the magnetic tunnel junction memory is connected between the first terminal of the first switch and the first terminal of the second switch.

7. The MRAM memory array as claimed in claim 1, wherein the first switch and the second switch are NMOS transistors.

8. The MRAM memory array as claimed in claim 1, wherein the number of word lines is three and the number of bit lines is two.

9. The MRAM memory array as claimed in claim 1, wherein the numbers of word lines is three and the number of bit lines is three.

10. An MRAM memory array, comprising:

word lines;

bit lines crossing the word lines;

first diodes, each first diode comprising:

a cathode; and

an anode coupled to a corresponding bit line;

second diodes, each second diode comprising:

an anode; and

a cathode coupled to a corresponding word line; and

magnetic tunnel junction memories including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer and the free layer;

each magnetic tunnel junction memory being positioned at a crossing point of a bit line and a word line, each magnetic tunnel junction memory being connected between a

first diode at a corresponding crossing bit line and a second diode at a corresponding crossing word line.

11. The MRAM memory array as claimed in claim 10, wherein the number of diodes is equal to the total number of word lines and bit lines.

12. The MRAM memory array as claimed in claim 10, wherein the number of magnetic tunnel junction memories is the product of the number of word lines and the number of bit lines.

13. The MRAM memory array as claimed in claim 10, wherein the numbers of word lines is three and the numbers of the bit lines is two.

14. The MRAM memory array as claimed in claim 10, wherein the numbers of word lines is three and the number of bit lines is three.

15. AN MRAM memory array, comprising:

a global word line;

a global bit line;

a first word line;

a second word line;

a third word line;

a first bit line crossing the first word line, the first bit line further crossing the second word line, the first bit line further crossing the third word line;

a second bit line crossing the first word line, the second bit line further crossing the second word line; the second bit-line further crossing the third word line;

a first switch having:

a first terminal;

a second terminal coupled to the first bit line; and

a control gate coupled to the global word line;

a second switch having:

a first terminal;

a second terminal coupled to the second bit line; and

a control gate coupled to the global word line;

a third switch having:

a first terminal;

a second terminal coupled to the first word line; and

a control gate coupled to the global bit line;

a fourth switch having:

a first terminal;

a second terminal coupled to the second word line; and

a control gate coupled to the global bit line;

a fifth switch having:

a first terminal;

a second terminal coupled to the third word line; and

a control gate coupled to the global bit line;

a first magnetic tunnel junction memory connected between the first terminal of the first switch and the first terminal of the third switch, the first magnetic tunnel junction memory including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer of the first magnetic tunnel junction memory and the free layer of the first magnetic tunnel junction memory;

the first magnetic tunnel junction memory being positioned at a crossing point of the first bit line and the first word line;

a second magnetic tunnel junction memory connected between the first terminal of the second switch and the first terminal of the third switch, the second magnetic tunnel junction memory including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer of the second magnetic tunnel junction memory and the free layer of the second magnetic tunnel junction memory;

the second magnetic tunnel junction memory being positioned at a crossing point of the second bit line and the first word line;

a third magnetic tunnel junction memory connected between the first terminal of the first switch and the first terminal of the fourth switch, the third magnetic tunnel junction memory including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer of the third magnetic tunnel junction memory and the free layer of the third magnetic tunnel junction memory;

the third magnetic tunnel junction memory being positioned at a crossing point of the first bit line and the second word line;

a fourth magnetic tunnel junction memory connected between the first terminal of the second switch and the first terminal of the fourth switch, the fourth magnetic tunnel junction memory including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer of the fourth magnetic tunnel junction memory and the free layer of the fourth magnetic tunnel junction memory;

the fourth magnetic tunnel junction memory being positioned at a crossing point of the second bit line and the second word line;

a fifth magnetic tunnel junction memory connected between the first terminal of the first switch and the first terminal of the fifth switch, the fifth magnetic tunnel junction memory including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer of the fifth magnetic tunnel junction memory and the free layer of the fifth magnetic tunnel junction memory;

the fifth magnetic tunnel junction memory being positioned at a crossing point of the first bit line and the third word line; and

a sixth magnetic tunnel junction memory connected between the first terminal of the second switch and the first terminal of the fifth switch, the sixth magnetic tunnel junction memory including:

a pinned layer;

a free layer; and

a non-magnetic layer located between the pinned layer of the sixth magnetic tunnel junction memory and the free layer of the sixth magnetic tunnel junction memory;

the sixth magnetic tunnel junction memory being positioned at a crossing point of the second bit line and the third word line.

16. The MRAM memory array as claimed in claim 15, wherein the first switch, the second switch, the third switch, the fourth switch and the fifth switch are NMOS transistors.

17. An MRAM memory array, comprising:

a first word line

a second word line;

a third word line;

a first bit line crossing the first word line, the first bit line further crossing the second word line; the first bit line further crossing the third word line;

a second bit line crossing the first word line, the second bit line further crossing the second word line; the second bit line further crossing the third word line;

a first diode having a first cathode, and a first anode coupled to the first bit line;

a second diode having a second cathode, and a second anode coupled to the second bit line;

a third diode having a third anode, and a third cathode coupled to the first word line;

a fourth diode having a fourth anode, and a fourth cathode coupled to the second word line;

a fifth diode having a fifth anode, and a fifth cathode coupled to the third word line;

a first magnetic tunnel junction memory connected between the first cathode and the third anode, the first magnetic tunnel junction memory including:

a first pinned layer;

a first free layer; and

a first non-magnetic layer located between the first pinned layer and the first free layer;

the first magnetic tunnel junction memory being positioned at a crossing point of the first bit line and the first word line;

a second magnetic tunnel junction memory connected between the second cathode and the third anode, the second magnetic tunnel junction memory including:

a second pinned layer;

a second free layer; and

a second non-magnetic layer located between the second pinned layer and the second free layer;

the second magnetic tunnel junction memory being positioned at crossing point of the second bit line and the first word line;

a third magnetic tunnel junction memory connected between the first cathode and the fourth anode, the third magnetic tunnel junction memory including:

a third pinned layer;

a third free layer; and

a third non-magnetic layer located between the third pinned layer and the third free layer;

the third magnetic tunnel junction memory being positioned at crossing point of the first bit line and the second word line;

a fourth magnetic tunnel junction memory connected between the second cathode and the fourth anode, the fourth magnetic tunnel junction memory including:

a fourth pinned layer;

a fourth free layer; and

a fourth non-magnetic layer located between the fourth pinned layer and the fourth free layer;

the fourth magnetic tunnel junction memory being positioned at crossing point of the second bit line and the second word line;

a fifth magnetic tunnel junction memory connected between the first cathode and the fifth anode, the fifth magnetic tunnel junction memory including:

a fifth pinned layer;

a fifth free layer; and

a fifth non-magnetic layer located between the fifth pinned layer and the fifth free layer;

the fifth magnetic tunnel junction memory being positioned at crossing point of the first bit line and the third word line; and

a sixth magnetic tunnel junction memory connected between the second cathode and the fifth anode, the sixth magnetic tunnel junction memory including:

a sixth pinned layer;

a sixth free layer; and

a sixth non-magnetic layer located between the sixth pinned layer and the sixth free layer;

the sixth magnetic tunnel junction memory being positioned at crossing point of the second bit line and the third word line.

18. An MRAM memory array comprising:

first and second buses associated with a plurality of first and second conductive lines, respectively;

a plurality of first and second switches, wherein each of the first switches couples the first bus to one of the second conductive lines and each of the second switches couples the second bus to one of the first conductive lines; and

a plurality of magnetic tunnel junction memories each positioned where one of the first conductive lines crosses one of the second conductive lines, wherein each of the plurality of magnetic tunnel junction memories is connected between a first switch at the corresponding second conductive line and a second switch at the corresponding first conductive line.

19. The MRAM memory array of claim 18 wherein each magnetic tunnel junction memories includes a pinned layer, a free layer, and a non-magnetic layer located between the pinned layer and the free layer.

20. The MRAM memory array of claim 18 wherein a total number of first and second switches is equal to a total number of first and second conductive lines.

21. The MRAM memory array of claim 18 wherein a total number of the magnetic tunnel junction memories is a product of a total number of first conductive lines and a total number of the second conductive lines.

22. The MRAM memory array of claim 18 further comprising a plurality of segments, wherein each segment includes at least two of the plurality of magnetic tunnel junction memories.

23. The MRAM memory array of claim 22 wherein the segments are separated by field effect transistors.

24. The MRAM memory array of claim 22 wherein the segments are separated by diodes.

25. A method for manufacturing an MRAM memory array, the method comprising:

forming first and second global buses connected the first and second to a plurality of first and second conductive lines, respectively;

forming a plurality of first and second switches, wherein each of the first switches couples the first global bus to one of the second conductive lines and each of the second switches couples the second global bus to one of the first conductive lines;

forming a plurality of magnetic tunnel junction memories, wherein each magnetic tunnel junction memory is positioned where one of the first conductive lines crosses one of the second conductive lines; and

connecting each of the plurality of magnetic tunnel junction memories between a first switch at the corresponding second conductive line and a second switch at the corresponding first conductive line.